REMARKS

By this amendment, claims 1, 3-16 and 18-32 are pending, in which claims 2 and 17 are canceled without prejudice or disclaimer, claims 1, 3, 5, 6, 16, 20, 21 and 32 are currently amended, and claim 33 is newly presented. No new matter is introduced.

The Office Action mailed June 27, 2006 rejected claims 1, 16, 31 and 32 under 35 U.S.C. § 102 as anticipated by *Chang et al.* (MEDIC: A Memory and Disk Cache for Multimedia Client), claims 2-7, 10, 17-22 and 25 as obvious under 35 U.S.C. § 103 based on *Chang et al.* in view of *Baldwin et al.* (US 7,050,061), and claims 8, 9, 11-15, 23, 24 and 26-30 as obvious under 35 U.S.C. § 103 based on *Chang et al.* in view of *Lemmons et al.* (US Pub. 2001/0013126).

In the interest of advance prosecution, Applicants have amended independent claims 1, 16 and 32 to include the features of dependent claim 2. For example amended independent claim 1 recites "said **MMU is configured** to translate a virtual address provided by said application to a physical address used by one of said physical memory and said bulk storage device, and **to page pages of said data stored in said physical memory to and from said bulk storage device.**"

The Office Action, on page 4, acknowledges that the base reference of *Chang et al.* lacks disclosure of these features. Accordingly, the Office Action is forced to rely on *Baldwin et al.* for such a supposed teaching, citing col. 3, lines 62-67 and col. 23, lines 53-67. Applicants respectfully disagree that the claimed features are taught by *Baldwin et al.* The cited passages state the following (Emphasis Added):

> The net effective speed of a large **DRAM memory** can be increased by using bank organization and/or page mode accesses; but such features can still provide only a limited speed improvement, and net effective speed of a large **DRAM memory** (as seen by the processor) will still typically be much slower than that of the processor. [col. 3: 62-67]
>
> The logical page the logical address resides in is calculated and the Translation Look aside Buffer (TLB) checked to see if the physical page assigned to the logical page is present. If it is the physical address is formed from the physical

> page number and the low order bits of the logical address. Note the physical page is relative to the start of the working set and not physical memory. The physical address is then posted to the memory controller. If the logical page is not present in the TLB then the Logical Page Table entry for this logical page is read. If the resident bit is set then the logical page is present in the working set and its physical page is read from the Logical Page Table. The TLB is updated so the next time this logical page is accessed the physical page is to hard. [col. 23: 53 – col. 24: 1]

At best, the above passages teach that bank organization and/or page mode accesses increases the net effective speed of a large DRAM. DRAM (Dynamic Random Access Memory) is a type of random access memory, and thus is distinguishable from the claimed bulk storage device.

Also, these passages are silent with respect to any teaching of "to page pages of said data stored in said physical memory to and from said bulk storage device." Instead, *Baldwin et al.*, within col. 3: 48-59, explains that their invention is largely irrelevant to virtual memory operation:

> In a virtual memory system, an arbitrary address may correspond to a physical location which is in main memory or mass storage (e.g. disk). In such systems, address translation performs fetches from mass storage if needed, transparently to the CPU. Virtual memory management, like cache management, is an important architectural design choice, and "memory management" logic often performs functions related to virtual memory management as well as to cache management. However, **the needs and impact of virtual memory operation are largely irrelevant to the disclosed innovations, and will be largely ignored in the present application.)**

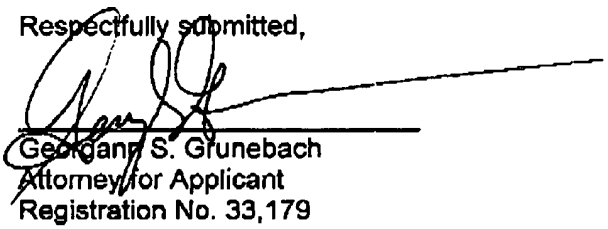
Furthermore, the Examiner is reminded that a prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. ***W.L. Gore & Associates, Inc. v. Garlock, Inc.***, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984).

In view of the foregoing, Applicants respectfully request withdrawal of the rejections under §§ 102 and 103.

Turning now to newly added claim 33, this independent claim is drawn to a method for storing a program guide, and recites "accessing a virtual memory page associated with the program guide; obtaining a virtual address corresponding to the virtual memory page; translating the virtual address to a physical address; determining whether the physical address is mapped to a physical page in a volatile memory; generating a page fault if no physical address is mapped to the physical page; determining whether to replace the physical page using a least-recently-used scheme; determining whether the physical page to be replaced has been updated; and if no update is determined, freeing a page within the volatile memory and mapping another virtual memory page to the corresponding freed page within the volatile memory, wherein a corresponding page in a hard disk is stored in location of the freed page." Applicants submit that the applied art, alone or in combination, does not satisfy all the claimed features. Hence, new claim 33 should be allowable.

Therefore, the present application, as amended, overcomes the rejections of record and is in condition for allowance. Favorable consideration of this application is respectfully requested. If any unresolved issues remain, it is respectfully requested that the Examiner telephone the undersigned attorney at (310) 964-4615 so that such issues may be resolved as expeditiously as possible. All correspondence should continue to be directed to our below-listed address.

Respectfully submitted,



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